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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,084	07/31/2003	Gerard Chauvel	TI-35428	2214

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
05/12/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/632,084	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/31/03,9/22/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 10-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 10 is directed toward a method of executing a test and skip instruction, comprising: calling the test and skip instruction within a sequence of instructions; examining a bit in the test and skip instruction; determining an address mode based on said bit; comparing contents of a first register of contents of a second register if the bit is in a first state; or comparing the contents of the first register to contents of a non-register location if the bit is in a second state; and skipping a subsequent instruction based on results of the comparison.

The test of whether a method claim is statutory is the machine or transformation test (e.g., see In re Bilski 88 USPQ 2d 1385). As to the machine portion of the test, the method of claim 10 is not associated with any particular machine. Note none of the steps of the method are performed by any particular machine. As to the transformation portion of the test, claim 10 does not transform any matter. Therefore Claims 10 fails the machine or transformation test and therefore is directed toward non-statutory subject matter. Claims 11 and 12 that depend from claim 10 are directed to non-statutory subject matter for the same reasons as claim 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 13-17, and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magoshi (patent No. 6,988,187) in view of Kusiak (patent No. 5,434,986).

Magoshi taught (As to claims 1, 13) the invention as claimed including A processor (e.g., see fig. 1, 6) executing a plurality of instructions (e.g., see fig. 5) comprising: an arithmetic logic unit(106, 252); and; wherein said processor executes a test and skip instruction when called within the plurality of instructions (e.g., see col. 7, lines 1-46) , compare values and to execute or not execute a subsequent instruction that follows the test and skip instruction based on the comparison(e.g., see col.7, lines 13-46). Magoshi did not expressly detail a plurality of registers coupled to the ALU, each register programmable to store a register value that includes a first register reference and a second register reference that causes the processor to compare first value comprising stored in a register corresponding to the register reference and a second value associated with the second register reference. Kusiak however taught this limitation (e.g., see fig. 4, element 100 is a general register stack which is coupled to arithmetic logic unit 102) [in figures 10,11, and 12 when a skip instruction is encountered a test of whether the register reference values are equal is made for determining whether to skip a next instruction, e.g., see col. 11, lines 20-65].

Due to similarities of claims 1 and 13, claim 13 is rejected for the same reasons as claim 1 above. The ALU in claim 1 corresponds the main processor in claim 13 and coprocessor in claim 13 corresponds to the skip execution unit in fig. 3, 6 of Magoshi where the features of the coprocessor are rejected above in the discussion of the operation of the processor when it executes a test and skip instruction.

It would have been obvious to one or ordinary skill in the DP art to combine the teachings of Magoshi and Kusiak. Both references were directed toward the problems of implementing a skip instruction in a DP system. One of ordinary skill would have been motivated to incorporate the Kusiak teachings of accessing register values for comparison at least to provide for quick access to the comparison values in processing the skip instruction in a pipelined architecture. Also the addition of the Kusiak teachings would have yielded predictable results.

As to claims 2,14 Kusiakl taught wherein the second value comprises a register value stored in the second register reference (e.g., see col. 2, lines 20-65).

As to claims 3,15 Kusiak taught wherein the processor is configured to access memory and the second value is stored in the memory (e.g., see fig. 8)[in fig. 8 Kusiak taught the alternative embodiment where the branch instruction target is determined depending comparison of data accessed from memory (e.g., see col. 10 , lines 24-45) and that the skip instruction is a special case of the branch instruction (e.g., see col. 11, lines 31-36).

As to claim 4, 16 Kusiak taught wherein the second register reference contains a value used to compute a pointer to a memory location containing the second value (e.g., see col. 9, line 64-col. 10, line 45 and col. 7, lines 15-55).

As to claim 5,17 Kusiak taught wherein the pointer is computed by adding the value from the second register reference (B0) to a register value from another register(238) (e.g., see col. 9, line 64-col. 10, line 45 and col. 7, lines 15-55).

As to claim 22 Magoshi taught A programmable logic device (e.g., see figs. 1,6) comprising: control logic (106,252); and means for executing a test and skip instruction(102) when called within a sequence of instructions(e.g., see col. 7, lines 1-46) , compare values and for executing or not executing a subsequent instruction that follows the test and skip instruction based on the comparison (e.g., see col.7, lines 13-46). Magoshi did not specifically detail a first register reference identifying a first register having a register value and second register reference identifying a second reference also having a register value, for comparing a first value comprising the register value stored in the first register and a second value associated with the second register. Kusiak however taught this limitation (e.g., see fig. 4, element 100 is a general register stack which is coupled to arithmetic logic unit 102)[in figures 10,11, and 12 when a skip instruction is encountered a test of whether the register reference values are equal is made for determining whether to skip a next instruction, e.g., see col. 11, lines 20-65].

It would have been obvious toe one or ordinary skill in the DP art to combine the teachings of Magoshi and Kusiak. Both references were directed toward the problems

of implementing a skip instruction in a DP system. One of ordinary skill would have been motivated to incorporate the Kusiak teachings of accessing register values for comparison at least to provide for quick access to the comparison values in processing the skip instruction in a pipelined architecture. Also the addition of the Kusiak teachings would have yielded predictable results.

As to claim 23 Kusiak taught said second value is stored in a register (e.g., see col. 2, lines 20-65). .

As to claim 24 Kusiak taught wherein the processor is configured to access memory and the second value is stored in the memory (e.g., see fig. 8)[in fig. 8 Kusiak taught the alternative embodiment where the branch instruction target is determined depending comparison of data accessed from memory (e.g., see col. 10 , lines 24-45) and that the skip instruction is a special case of the branch instruction (e.g., see col. 11, lines 31-36).

As to claim 25 Kusiak taught wherein said second value stored in a stack (100,115)(e.g., see fig. 4 and col. 6, lines 40-67).

Claims 6-9,18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magoshi and Kusiak as applied to claims 1-5,13-17 above, and further in view of Catherwood (patent application publication No. 2003/0061464) .

As to claim 6 Catherwood taught wherein the value held in another register is post-incremented by a predetermined value following execution of the test and skip instruction(e.g., see page 7 and page 318 and pages 457-459)[addressing mode 1 and mode 2 and mode 3 each include post increment and these are modes for processing the branch and skip instructions] .

As to claims 7,18 Catherwood taught wherein the comparison includes a condition that is specified in the test and skip instruction(e.g., see pages 138-139).

As to claims 8,19 Catherwood taught wherein any of a plurality of conditions are specified in the test and skip instruction(e.g., see pages 138-139,pages 80-81)(skip if bit is set or alternatively skip if specified bit set where the first bit in the third filed from right in the instruction encoding provides indication of the condition to be tested see page 80-81).

As to claims 9 ,20 Catherwoood taught wherein the condition is a condition selected from the group consisting of equal to, not equal to, less than,(e.g., see pages 59,60,80,81 and 138-139 and greater than with branch instruction instructions where some specifically included skip operations (e.g., see page 61where branch if negative provides branch if less than zero). Also,Kusiak taught that skip instructions were a special case of branching (e.g., see col. 3, lines 56-67). Therefore one of ordinary skill would have been motivated to include the less than condition for skip instruction as skip instructions are subset of branch instructions as taught by Kusiak and Catherwood taught using the less than condition for branching. This would have provided the combined system the similar increased flexibility provided for determining a condition

was met when skip branch instructions as when the non-skip branching instructions were executed.

As to claim 21 Catherwood taught the applications for the system were soft modem speech recognition etc. (e.g., see paragraphs 0008-0009). Therefore one of ordinary skill would have been motivated to implement the combined system wherein the system comprises a communication device at least to implement the input/output required for applications such as speech recognition or soft modem etc.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Perry (patent No. 6,880,074) disclosed in-line code suppression (e.g., see abstract).

Ellis(patent No. 6,029,226) disclosed system having automated write data transfer with optional skip by processing two write commands as a single write command (e.g., see abstract).

Mennemeier (patent No. 5,642,306) disclosed system for a single instruction multiple data early-out zero-skip multiplier (e.g., see abstract).

Lucas (patent No. 5,644,759) disclosed system for processing a jump instruction preceded by a skip instruction (e.g., see abstract).

Ohara (patent No. 6,047,366) disclosed single-instruction multiple-data processor with input and output registers having a sequential location skip function (e.g., see abstract).

Nukiyama (patent No. 4,926,312) disclosed Program skip operation control (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

/Eric Coleman/
Primary Examiner, Art Unit 2183